27. (Amended) The RF passive circuit of Claim 7, wherein the wiring metal layer is formed by an evaporation process.

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28. (Amended) The RF passive circuit of Claim 7, wherein the inside end of the wiring metal layer is connected to the via-hole by a ground layer over one end of the via-hole on the semiconductor substrate.

REMARKS

Claims 7, 9, 27, and 28 remain in this application. Applicant respectfully requests re-examination.

Claims 7, 9, 27, and 28 were rejected under 35 U.S.C. Section 112 for reciting "the first wiring metal layer and the wiring metal layer". Claims 7, 9, 27, and 28 have been amended to eliminate the lack of antecedent basis and ambiguity pointed out for these claims in the office action. Applicant respectfully requests that this rejection be withdrawn.

Claims 7, 9, 27, and 28 were rejected under 35 U.S.C. Section 102(b) as anticipated by the prior art described by applicant in Figures 8A-8D. Applicant respectfully traverses.

Both independent Claims 7 and 9 specifically recite "a wiring metal layer formed in a spiral pattern with an inside end on the semiconductor substrate, the wiring metal layer being electrically connected to the via-hole at the inside end; an inductor of metal film formed in a spiral pattern with an inside end on the wiring metal layer, with the inside end of the inductor film being near the via-hole".

Figures 8A-8D of the application do not show and the application does not describe such a structure. The Figures 8A-8D of the application show the inductor in a spiral pattern. However, the wiring metal layer is in a linear form. The resulting capacity between the inductor

and the wiring metal layer will not be as great as the capacity generated by the claimed spiral wiring metal layer and spiral inductor metal film. The claimed invention thus increases mounting density by providing a sufficient capacity in a smaller space than is possible by the structure shown and described in Figures 8A-8D of the application. Applicant respectfully requests that this rejection be withdrawn.

Claim 8 was rejected under 35 U.S.C. Section 103(a) as unpatentable over Applicant's admitted prior art in view of U.S. Patent No. 6,075,427 (Tai, et al.). Applicant respectfully traverses.

Tai, et al. discloses first and second spiral-shaped layers 26, 28 which are connected at their inner conductor portions 32, 36 by a via-hole 38 which extends between the spiral-shaped layers 26, 28 through a dielectric layer 44, as shown in Figures 3 and 4 (Col. 3, Lines 35-41).

Applicant's claimed structure, the spiral wiring metal layer and the spiral inductor metal film, rather than being located on opposite sides of a dielectric layer and connected together by a via-hole, are located on the same side of a semiconductor substrate and connected to a via-hole through the semiconductor substrate. The formed circuit element on the semiconductor substrate is connected to the remaining elements mounted on the semiconductor substrate through this via-hole.

The dielectric layer, as claimed in Claims 7 and 9, is located only between the spiral wiring metal layer and the spiral inductor metal film. The dielectric layer 44 of Tai, et al. is a layer deposited on both the first spiral-shaped layer 26 of Tai and the SiO_2 layer 42. The second spiral-shaped layer 28 of metallic material is deposited on the dielectric layer 44, thus requiring a via hole in the dielectric layer 44 to connect the inner connector portion 32 of the first spiral-shaped

layer 26 and the inner connector portion 36 of the second spiral-shaped layer 28 together (Col. 3, Lines 51-67).

Applicant's via-hole connects the formed RF passive circuit element to the rest of the components on the semiconductor substrate. Tai's via-hole connects the two inner ends of his first spiral-shaped layer and second spiral-shaped layer.

Applicant respectfully requests that the above rejection be withdrawn.

In light of the above amendment and remarks, Applicant believes that this case is condition for allowance and respectfully requests that it be passed to issue.

I hereby certify that this correspondence is being sent First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on October 4, 2002.

By: Marc Fregoso

Signature

Date: October 4, 2002

Respectfully submitted,

PRICE AND GESS

Albin H. Gess
Registration No. 25,726
2100 S.E. Main St., Suite 250
Irvine, California 92614
Telephone: 949/261-8433

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Kindly cancel Claim 8 without prejudice.

7. (Amended) An RF passive circuit comprising:

a semiconductor substrate;

a via-hole [which is formed by applying a metal film on an inside wall of a hole provided] through the semiconductor substrate, the via-hole having a metal film on an inside wall;

a wiring metal layer [which is] formed in a spiral pattern with an inside end on [a main surface of] the semiconductor substrate [and is] , the wiring metal layer being electrically connected to the via-hole at the inside end; [and]

an inductor [which is made] of [a] metal film formed in a spiral pattern with an inside end [and is formed] on the [first] wiring metal layer with the inside end of the inductor film being near the via-hole; and

a dielectric layer between the spiral wiring metal layer and the spiral inductor metal film [therebetween].

9. (Amended) An RF choke used in at least one of a matching circuit and a bias feeding circuit, both circuits being included in an RF amplifier, the RF choke comprising:

a semiconductor substrate where at least one of the matching circuit and the bias feeding circuit is incorporated;

a via-hole [which is formed by applying a metal film on an inside wall of a hole provided] through the semiconductor substrate, the via-hole having a metal film on an inside wall;

a wiring metal layer [which is] formed in a spiral pattern with an inside end on [a main surface of] the semiconductor substrate [and is] , the wiring metal layer being electrically connected to the via-hole at the inside end; [and]

an inductor [which is made] of [a] metal film formed in a spiral pattern with an inside end [and is formed] on the [first] wiring metal layer with the inside end of the inductor film being near the via-hole; and

a dielectric layer between the spiral wiring metal layer and the spiral inductor metal film [therebetween].

27. (Amended) The RF passive circuit of Claim 7, wherein the wiring metal layer is [evaporated in a spiral pattern] formed by an evaporation process.

28. (Amended) The RF passive circuit of Claim 7, wherein [the main surface has a first layer of an insulated film under the wiring metal layer and a second layer of a ground metal layer above the via-hole that connects] the inside end of the wiring metal layer [to the metal film of the via-hole] is connected to the via-hole by a ground layer over one end of the via-hole on the semiconductor substrate.